Design of a PFC Boost Converter Control Loop Using Smart Control and PSIM Software

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Abstract: Power Factor Correction (PFC) works by aligning the power supply's input current waveform with the line voltage waveform, thereby achieving the highest possible true power extraction from the electrical grid. Ideally, a PFC circuit would cause the input current to perfectly mimic the input voltage, behaving like an ideal resistive load with absolutely no harmonic distortion in the input current. This document outlines a systematic approach for designing a PFC Boost converter, offers guidelines for choosing the necessary semiconductor and passive components, and presents a practical design example complete with performance measurements. In the end, the effectiveness of the proposed plan and handling procedure is verified via simulation tests using PSIM and SMART/CTRL software. The simulation results show that the newer approach improves power flow for the embedded flyback micro-inverter compared to the standard power flow method.

Keywords: Boost converter, Power Factor Correction (PFC), current control, Smart Control

1 Introduction

There's a growing need for solid-state alternating current to direct current power conversion units. These devices find use across various sectors, including continuous power backup systems (UPSs), reserve energy reservoirs, charging equipment for electric and hybrid vehicles, power infrastructure for telecommunications equipment, and variable speed motor controllers (ASDs). Nevertheless, a drawback of these converters is that they pull non-smooth, pulsating current from the main power lines, leading to a suboptimal power factor. Furthermore, the high-frequency operation of the switching components causes the converters to contaminate the alternating current network by feeding substantial harmonic currents back into the grid. Addressing substandard power quality presents a substantial hurdle for both electricity distribution companies and manufacturers of power converters. A power factor correction (PFC) circuit proves effective in substantially lowering current harmonic content. Furthermore, utilizing a boost-type PFC converter allows for reduced electromagnetic interference (EMI) compared to alternative active PFC topologies when operating in continuous conduction

mode (CCM). Consequently, a majority of bridgeless designs currently utilized adopt the boost configuration (often termed dual-boost PFC rectifiers) due to their economic viability, combined with superior performance attributes like efficiency, power factor, and straightforwardness. Therefore, the objective of this project centers on developing a power factor correction solution based on a boost converter. [8]

SmartControl is a general-purpose software specifically devised for power electronics applications. This guide aims to lead you, step-by-step, to formulate the control loops of a PFC (power factor correction) boost converter with SmartControl software.

In Figure 1 underneath, the PFC assist converter circuit is evaluated based on PSIM software.

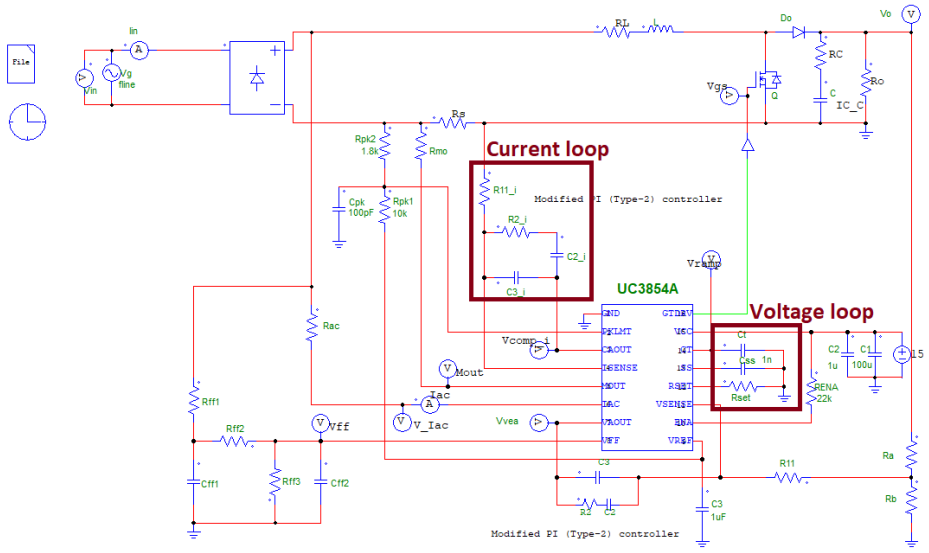

Fig. 1. Required PFC system

The circuit encompasses the inner current loop and the exterior voltage loop. The settings for the current loop regulator are the resistance R_{11}, R2_i and the capacitances C2_i, C3_i. and the settings for the voltage regulator are the resistance R_{set} and the capacitances C_{ss} and C_t, which are noted in the crimson boxes in Figure 1.

The aim of this piece is to devise present and electrical potential regulators employing SmartCtrl software. The devising sequence is detailed hereunder.

2 Starting the design process with SmartCtrl

For initiating the drawing procedure, in SmartCtrl, press the symbol shown at the peak of Figure 2 or select the toolbar symbol depicted at the base of Figure 2.

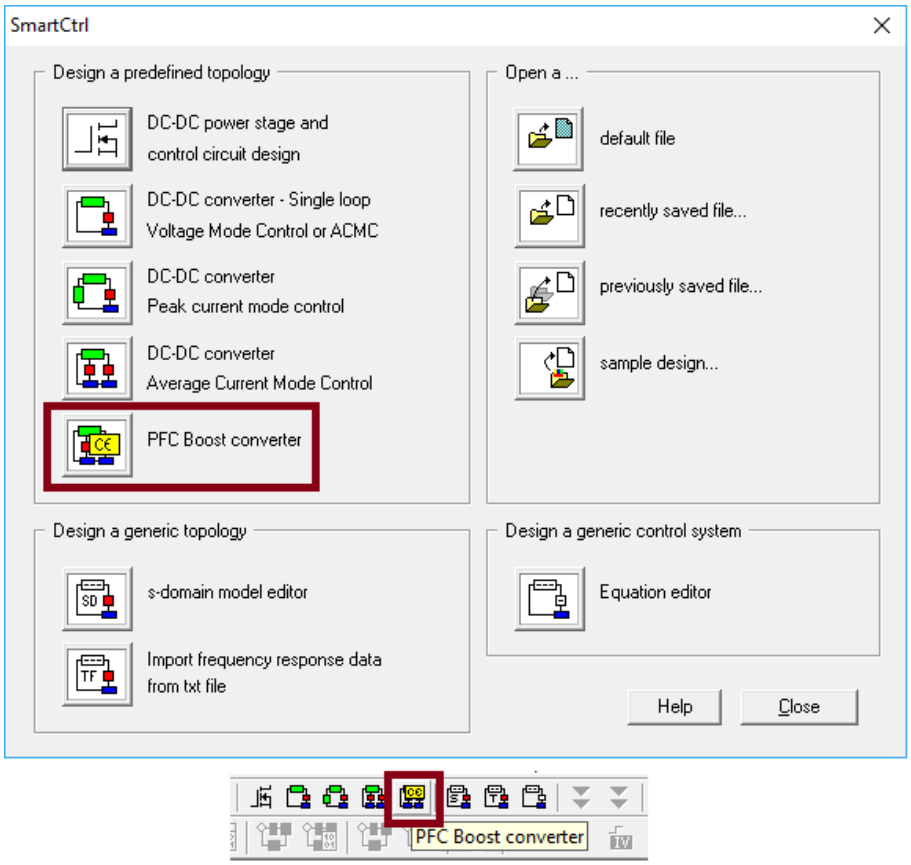

Fig. 2. Ways to access the PFC design guide

It can also be reached through the Design menu, Predefined Topologies >AC/DC Converters ->PFC Boost Converter. Whichever access is chosen, the window in Figure 3 will show.

On Figure 3, all fields are grouped based on whether they serve an inner or outer control loop.

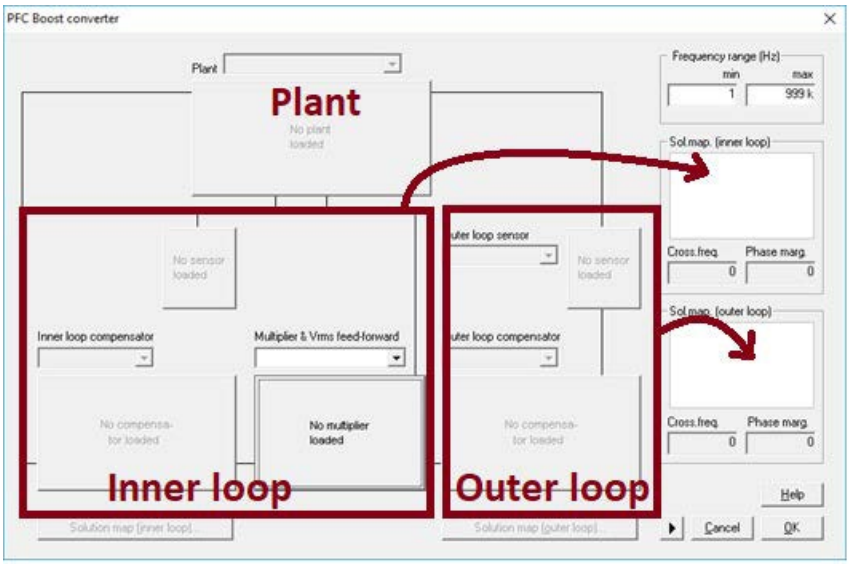

Fig. 3. PFC template structure

As depicted in Figure 3, the PFC boost converter is managed by a dual-loop control arrangement. The inner circuit is a current loop, and the external circuit is a voltage loop. Observe that the planning of the PFC boost converter needs to be executed step-by-step. The SmartCtrl software shall direct us throughout this procedure.

3 Inner loop design

Previoulsy designing the inner cycle, we select the fashion of multiplier.

1. We pick the UC3854A multiplier as shown in Figure 4

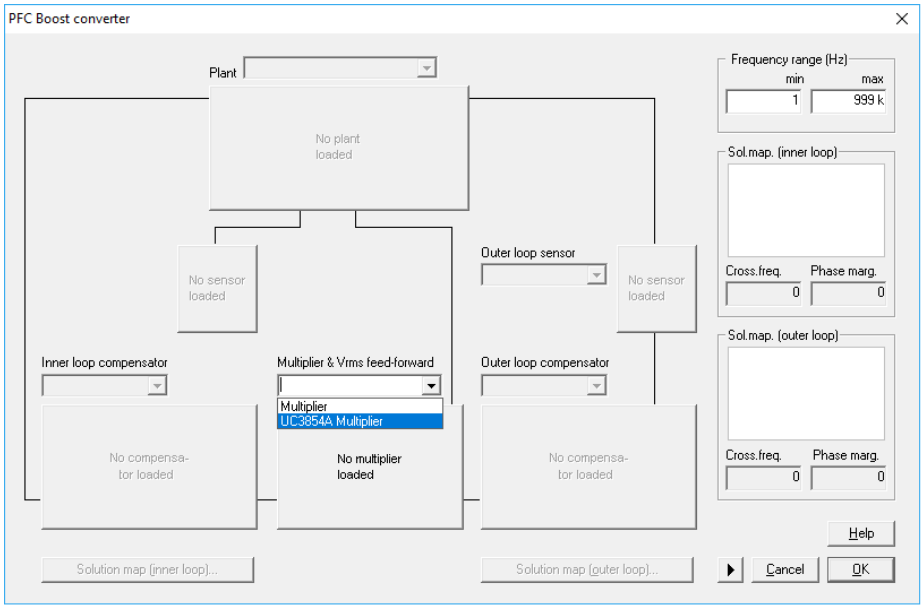

Fig. 4. Inner loop multiplier

Considering the circuit drawing of Figure 1, the multiplier settings for this specific case are those displayed in Figure 5.

We notice that KFF, the feed forward factor, is the proportion between the RMS input tension and the mean input tension to the multiplier. It has been computed that:

$$KFF = \sqrt{2} \times \frac{2}{\pi} \times \frac{RFF3}{RFF1 + RFF2 + RFF3} \quad [1]$$

Where RFF1, RFF2 and RFF3 constitute the resistors with the same designation that can be observed in the diagram of Figure 1.

The setup of the UC3854A multiplier is accomplished in this manner (figure 5). [9]

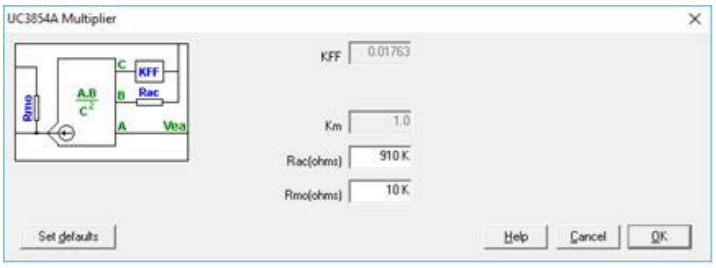

Fig. 5. UC3854 multiplier

2. We choose the gain of the inner loop current sensor (figure 6)

We pick the worth of the resistor that shall function as an amperage gauge (Rs). This resistor is shown in the visual of the power station.

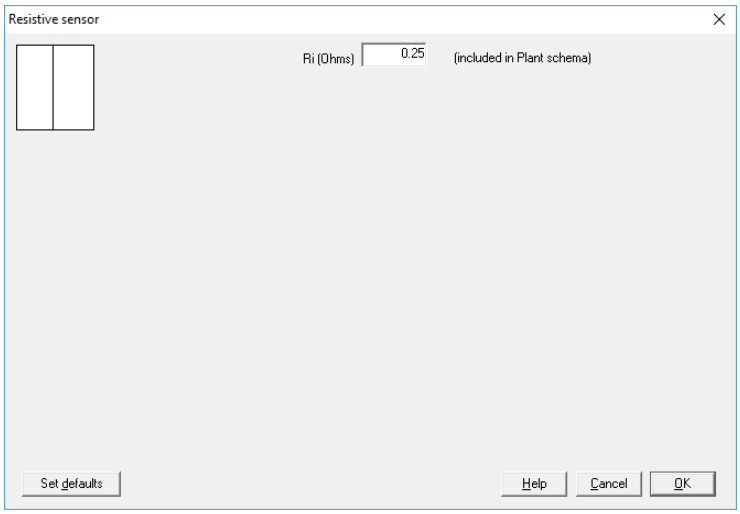

Fig. 6. Inner loop current sensor

3. At this juncture, the inner current circuit is largely delineated as depicted in Figure 7. To finalize this circuit, one must specify the layout of the setup. For this purpose, we choose a PFC boost unit (ohmic load).

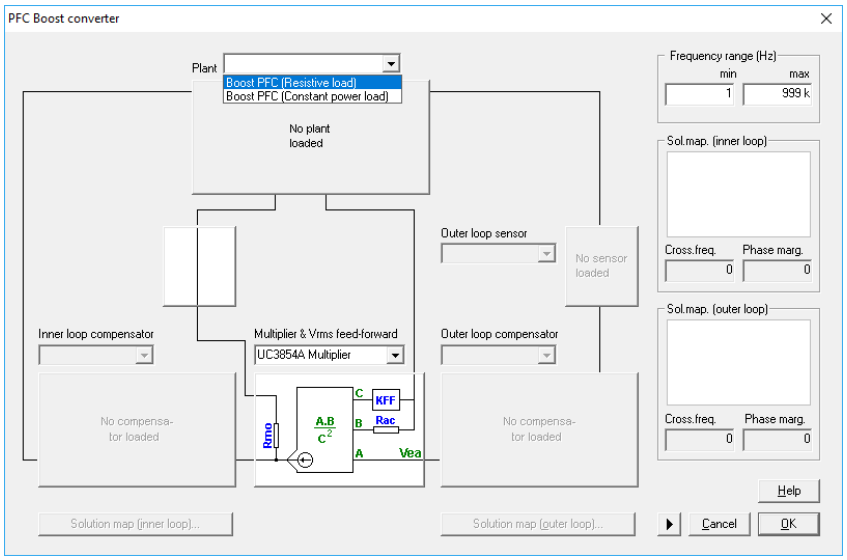

Fig. 7. The internal current loop is almost defined

4 Setting up the installation and the internal loop compensator

1. We choose the Boost PFC (Resistive load) configuration for the PFC boost converter. We input the parameters in the initial data window as demonstrated in Figure 8. Note that the input voltage is in RMS amount.

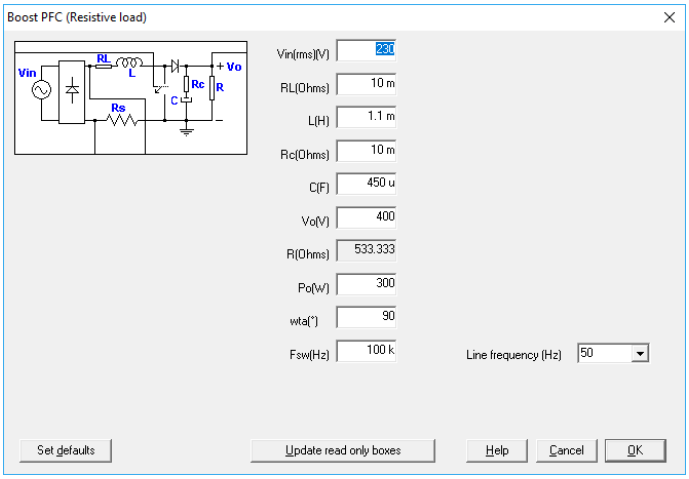

Fig. 8. Power plant parameters

Notarize that wta (º) is the angular measure in degrees whereon the operational point of the setup is determined. The existing circuit is devised bearing in mind the setup

computed for this operational position. This angular measure is designated as a crimson sphere in the resulting schedule depicting the yield of the corrected voltage and the external auxiliary.

2. We choose a Type 2 as the present regulator as shown in Figure 9 and set it up as done in Figure 10.

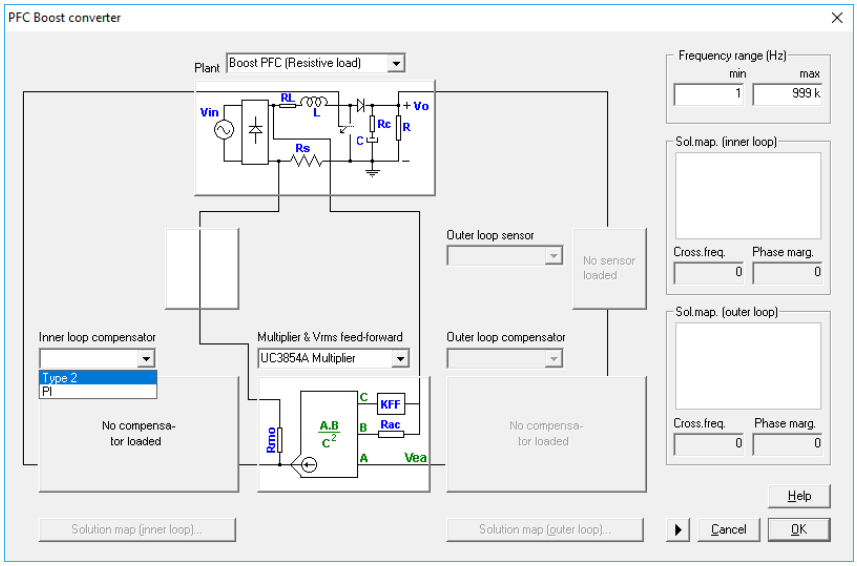

Fig. 9. Select a Type 2 for an inner loop setup

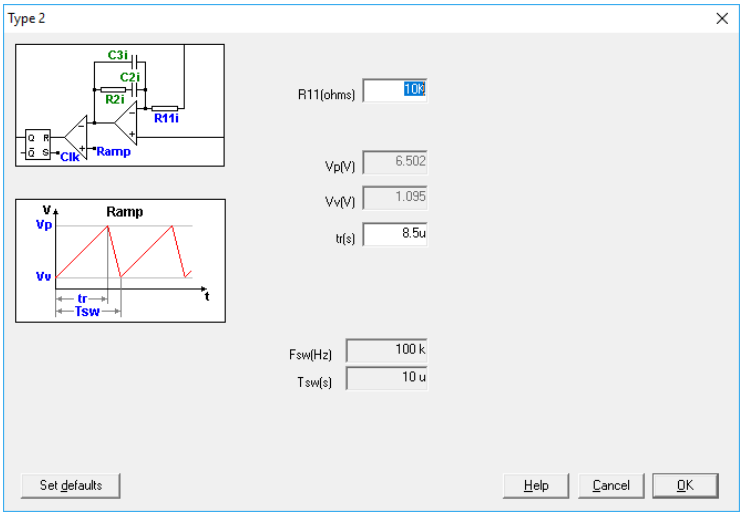

Fig. 10. Type 2 parameters

It is essential to comprehend the ramp waveform (Figure 10) to ascertain the parameters V_p (peak voltage), Vv (trough voltage), and t_r (ascend duration). These characteristics configure the converter modulator, whose amplification is significant for the computation of the inner circuit.

3. We choose the angular frequency and the phase margin with the help of the solution map (figure 11 and figure 12).

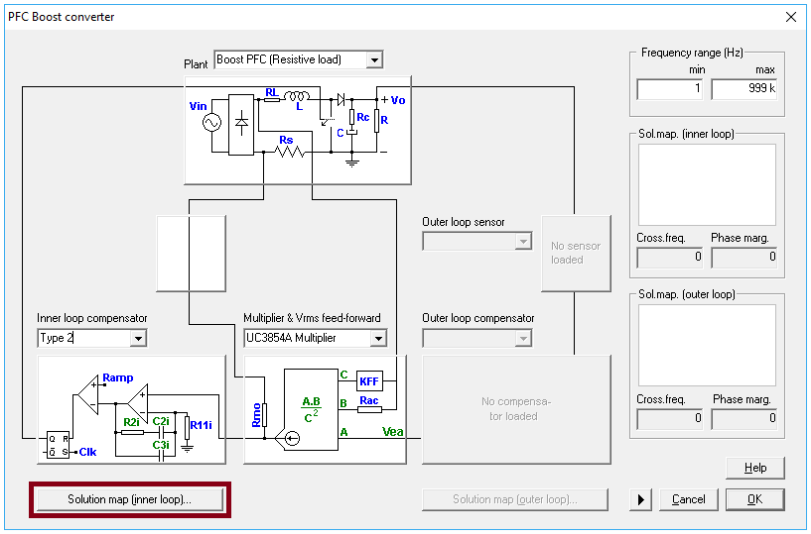

Fig. 11. Inner loop solution map access button

SmartCtrl furnishes a directive and a simple manner to pick the crossover frequency and phase margin through the Solution Map (figure 12).

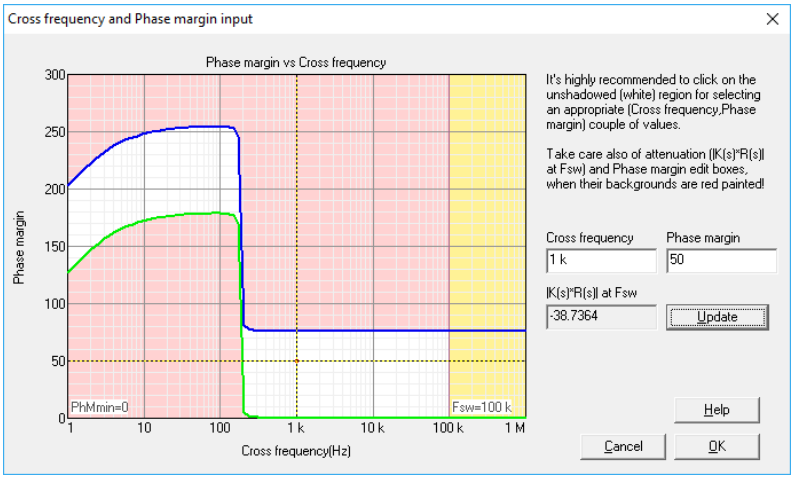

Fig. 12. Inner loop solution map

In the resolution map, each spot throughout the light region represents a mix of crossover recurrence and phase leeway that causes a reliable outcome. Moreover, once a spot is chosen, the dampening furnished by the detector and the controller at the switching recurrence is furnished.

For making the election, we tap on a spot inside the light region or that can be executed by hand by inputting the crossover recurrence and phase leeway and pressing refresh.

In this layout, a junction frequency of 1kHz and a Phase Margin of 50 degrees have been chosen. This pair of values will yield a reduction of -39dB at the switching frequency.

Once the junction frequency and phase margin are chosen, the solution layout will show up on the right side of the input screen of the converter. If, at any moment, we wish to alter the junction frequency or phase margin, we click on the white space of the Solution Map, as depicted in Figure 13.

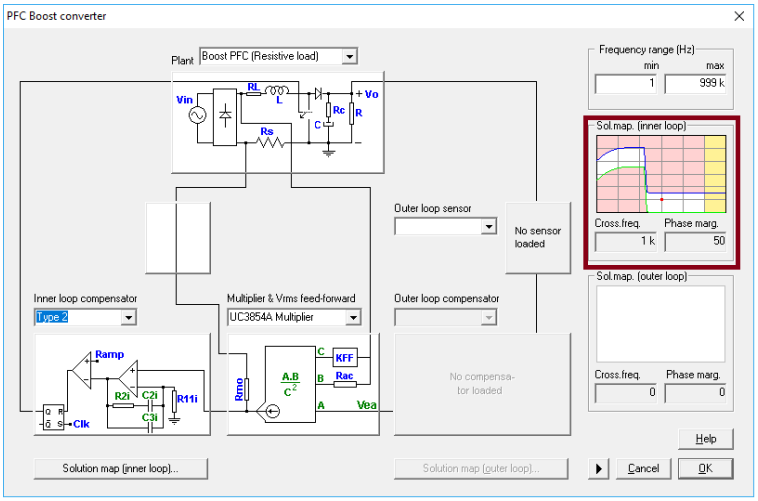

Fig. 13. Inner loop solution map shortcut access

5 Outer loop design

The procedure for conceiving the exterior circuit is quite analogous to that of the interior circuit.

1. We choose the voltage sensor. In this specific instance, the selection favored is "Built-in regulator voltage divider" (figure 14).
   We don't require setting any further specifications on this sensor.

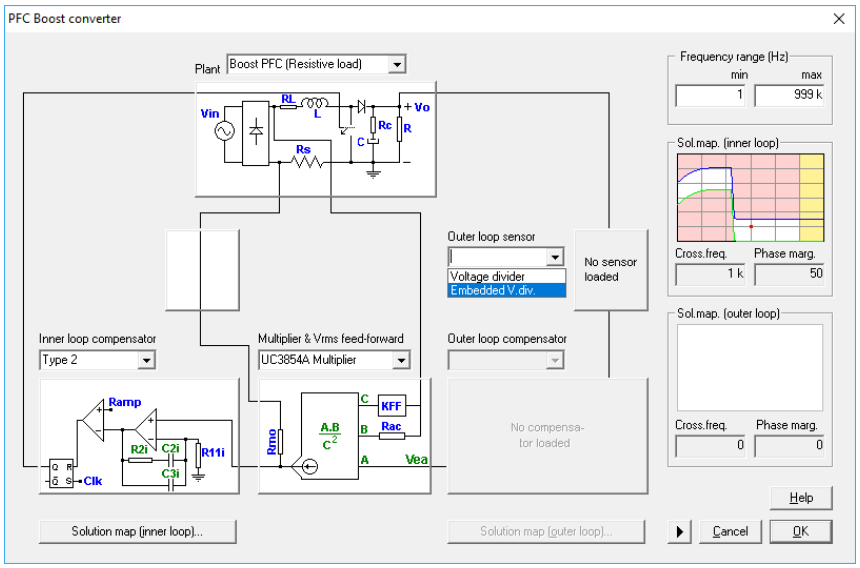

Fig.14. External loop sensor selection

2. We select the voltage regulator (Figure 15).

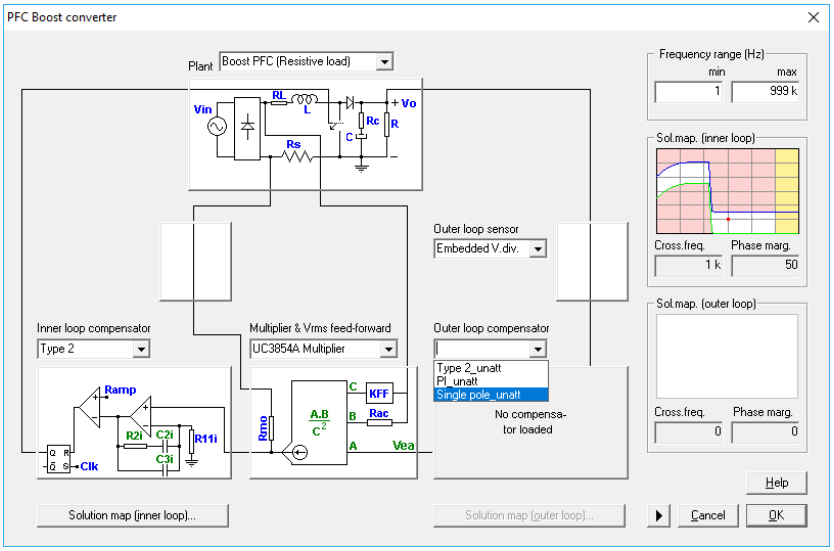

Fig. 15. Outer loop compensator selection

In this instance, the regulator kind is "Single pole unatt", with the specifications detailed in Figure 16.

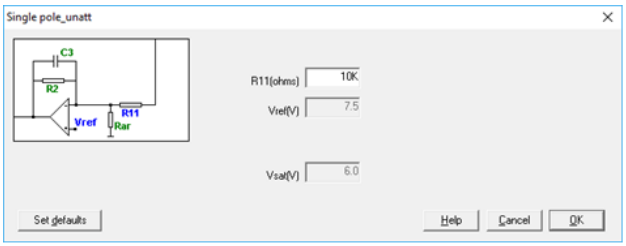

Fig. 16. Parameters of a unipolar outer loop compensator

In this situation, three distinct compensators may be employed:

a) PI Unattenuated – possesses infinite gain at DC thus will attain steady state magnitude. Nevertheless, it will introduce a slight alteration to the current shape which will lessen the Power Factor.
b) Type 2 non-attenuated – is rather analogous to non-attenuated PI and shares almost the same features.
c) Monopole – has limited gain at DC, consequently will not arrive at steady state output potential (will be some volts beneath the 400 V benchmark). However, it will not alter the current waveform, so is utilized when unity power factors are necessary.

3. We ascertain the crossover frequency and the phase margin.

The intersection frequency and phase allowance of the exterior circuit need to be chosen. An answer diagram is also offered to assist you in picking a steady resolution. We urge the Solution Map (exterior circuit) button (Figure 17) and the answer diagram will show up (Figure 18).

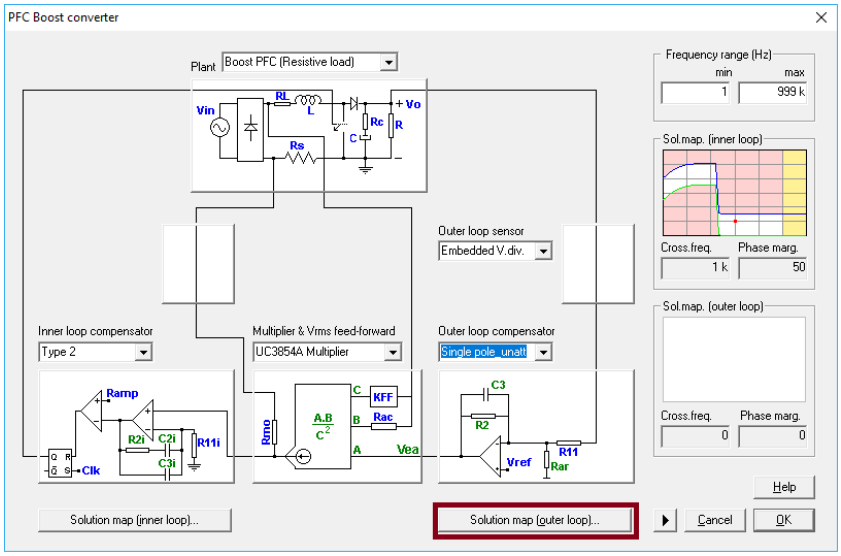

Fig. 17. Accessing the outer loop solution map

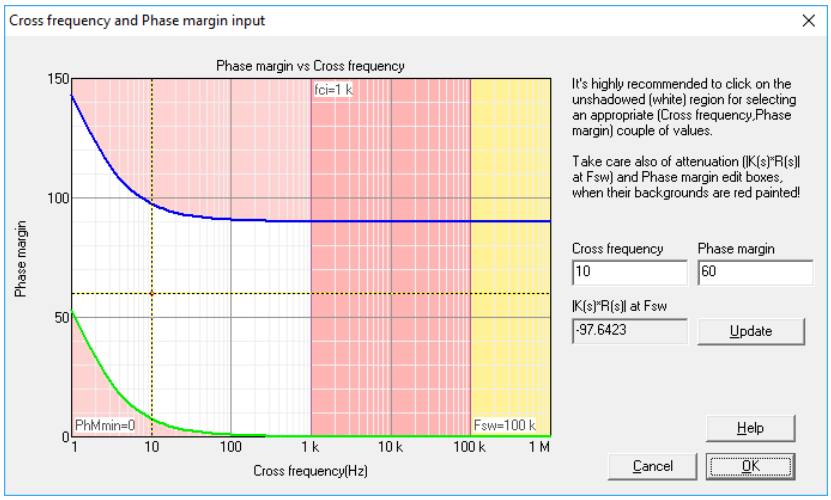

Fig. 18. Outer loop solution map

We chose a point by tapping the white sector and press OK to proceed. In this piece a crossover frequency of 10 Hz and a Phase Margin of 60 degrees were chosen.

After the crossover frequency and phase margin are picked, the Solution Map will show up on the right side of the input pane of the converter. If, at any instant, these two values must be altered, we merely tap on the white region of the Solution Map, as depicted in Figure 19.

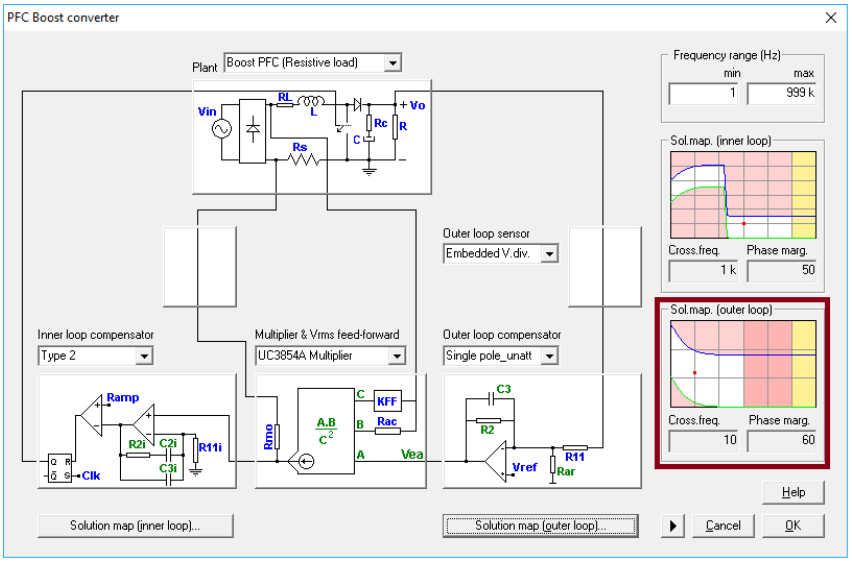

Fig. 19. Outer loop solution map shortcut access

4. We accept the selected design by clicking OK.

The main program shall spontaneously exhibit the computed control structure. Via BODE schematics, NYQUIST graphs, etc. its soundness and dynamic reaction might be verified.

6 Design results and interpretation

When the data entry assistant concludes, some tables surface so that we can examine the kinetic reaction of the currently configured control and fine-tune it. This window setup is depicted in Figure 21.

SmartCtrl offers various examination choices:

a) We examine the stable traces – they are depicted on the right. They prove quite helpful for spotting potential vibrations, interference, or signal shape alterations. For instance, should the PI compensator have been chosen for the external circuit, a flow disturbance would surface within these graphics (figure 21)
b) We verify the reaction to a minor signal step – It yields insight concerning the system's response, if it presents underdamping or overdamping (figure 21)
c) We examine the bandwidth with the graphs – The crossover frequency in the open loop is quite near to the closed loop bandwidth (figure 21)
d) We ascertain stability with the NYQUIST plot – it offers rapid-to-grasp data concerning the system's stability (figure 21)
e) We see the input and output reports (figure 20 and figure 22)
f) We perform a parametric scan (figure 20 and figure 23)
g) Alter input data for inner loop, outer loop and setup. (figure 20)
h) Illustration of data from an ingress or egress circuit. (figure 20)
i) Elaborate to PSIM. This feature has been covered in point 5

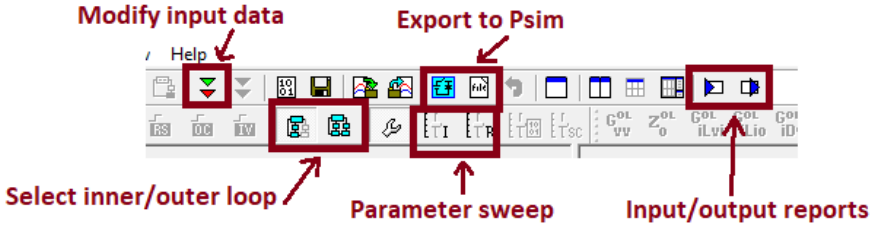

Fig. 20. SmartCtrl Basic Utilities

We observe that the solution map window is constantly active, so that the user perpetually possesses the capacity to alter the Phase Margin – crossover frequency pairing.

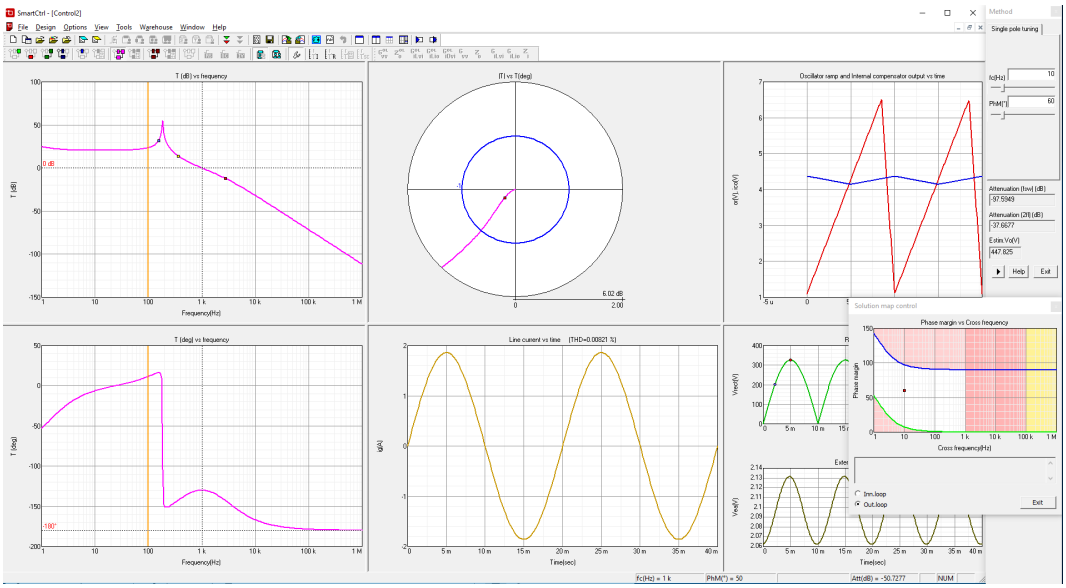

Fig. 21. SmartCtrl main window for inner loop

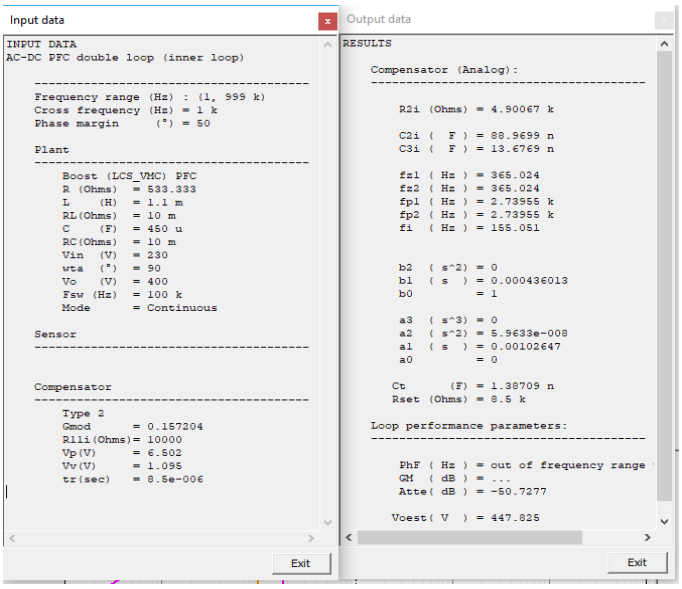

Fig. 22. Input/output data report

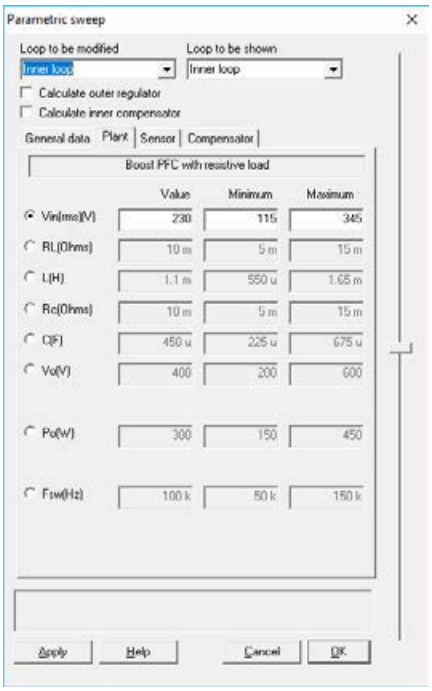

Fig. 23. Parametric scan of inner loop installation parameters

The Bode diagrams and Nyquist graph linked to the inner circuit are visible in Figure 21, and the visual data regarding the outer circuit is present in Figure 24. In the correct "Method" area, three variables are shown:

- **Atenuation (fsw) (dB).** This is the descrease in dB attained by the open loop transfer function at the switching frequency. It must be quite small for the inner and outer loops. Preferably lesser than -50dB.
- **Loop Gain (2fl) (dB).** This is the descrease in dB attained by the open loop transfer function at twice the line frequency (100 Hz or 120 Hz). It must be ample for the inner loop and little for the outer loop.
- **Vo (V).** As the outer loop compensator is unipolar, it lacks sufficient low frequency gain to attain the reference value. This is why SmartCtrl furnishes the output voltage value gotten with this compensator.

Advancing the mouse and pressing the right button upon the present line section reveals a pull-down listing presenting diverse selections. One of these constitutes the FFT directive, which exhibits a new pane with a chart illustrating the intensity of the initial and third overtones of the line flow, in the interest of conferring greater knowledge concerning the harmonic impurity. (Figure 25). [1]

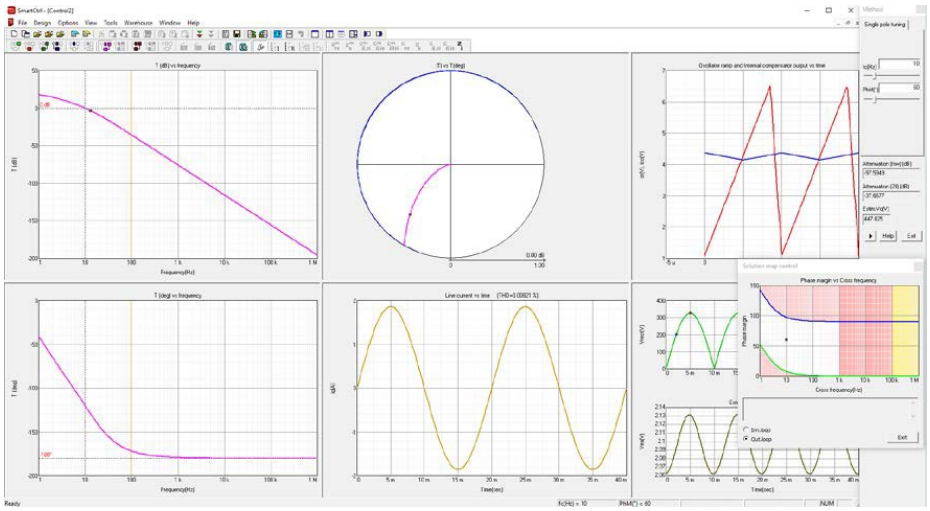

Fig. 24. SmartCtrl main window for the outer loop

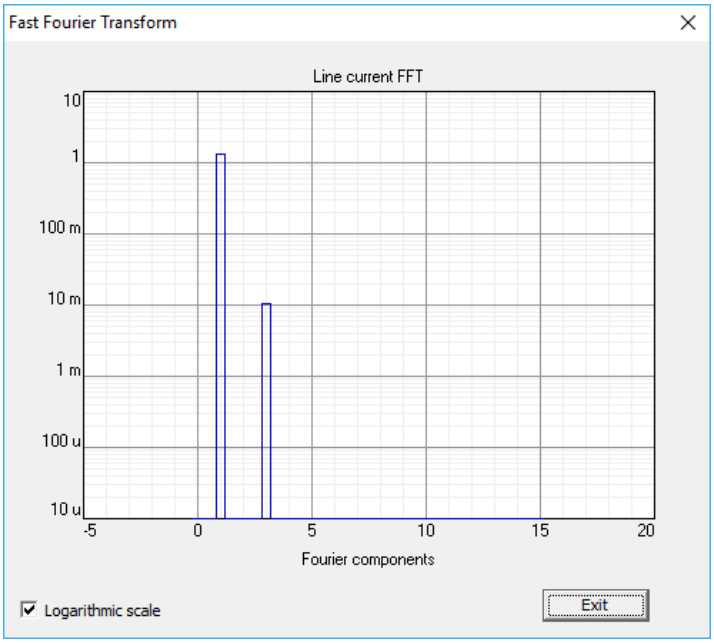

Fig. 25. Line current FFT 1st and 3rd harmonic

The crimson marking within the adjusted line voltage plot in Figure 26 primarily matches the line orientation wta detailed in the configuration pane (Figure 8). This marking can be shifted by pressing and pulling, and the Bode diagram and damping factors shall be revised as the setup is recomputed considering the equivalent DC/DC

apparatus for the designated operational spot. A sample is displayed in Figure 27, altering the line orientation. We notice how the closed circuit transmission functions.

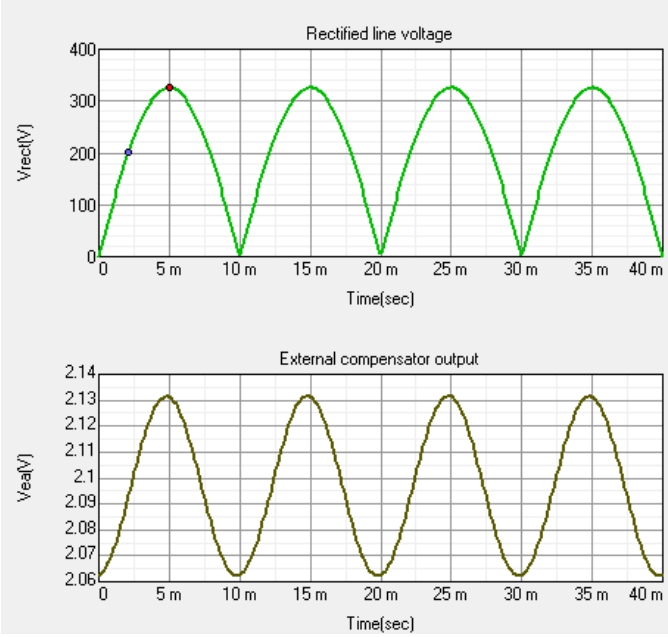

Fig. 26. Red dot representing the wta parameter

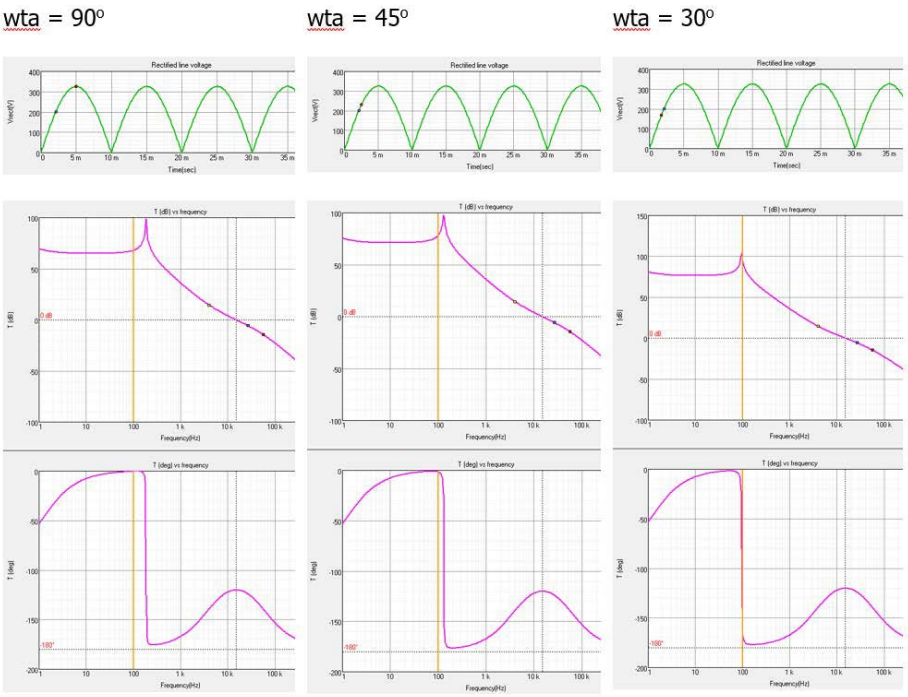

Fig. 27. WTA parameter scan and its effect on open loop

The azure sphere in the corrected line voltage representation (Figure 26) is situated at the line juncture corresponding to the peak current fluctuation through the choke. Certain outcomes derived from modeling the circuit schematic in Figure 1 are displayed in Figure 28.

For a demonstration of the significance of this azure point, the left section of Illustration 28 presents the voltage across the rectifier exit and the flow via the inductor, pointing out the position of the azure point.

On the right aspect of the drawing, a close-up of the same signals is exhibited, along with the oscillator incline and the outcome from the inner stabilizer.

The graph displaying the oscillator incline and the outcome from the inner stabilizer is handy in assessing if vibrations might exist. If the gradients of both features are alike, there could be above one crossing per cycle, leading to vibrations.

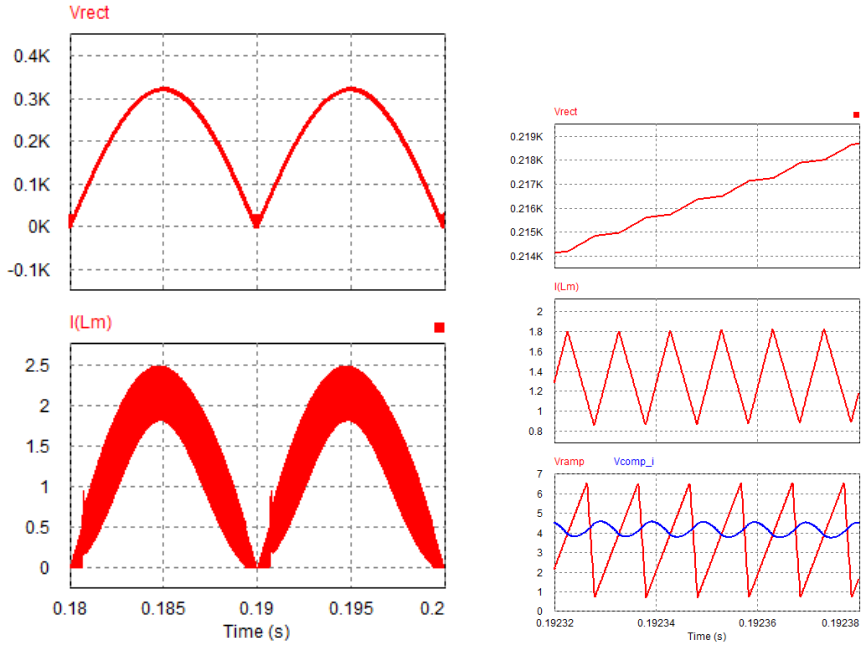

Fig. 28. Detail of the blue dot of the rectified line voltage view

When a unipolar type of external loop compensation is employed, there exist certain benefits regarding line current distortion. Conversely, the real output voltage might not precisely match what is specified due to the reduced gain at low frequency. This generates some discrepancies between the SmartCtrl outcomes and the simulated findings. Such an issue can be readily offset by the user through amplifying the output reference voltage.

Nonetheless, if the real output voltage is 10% taller than the determined, SmartCtrl shall present a caution notice, suggesting the operator to verify this aspect and augment the low frequency profit. In this illustration, the actual output voltage measures 415 V in place of the set 400 V, and consequently there exists no caution notice.

To demonstrate this issue pertaining to the reduced amplification of the exterior circuit at low periodicity, a novel outer loop was conceived, possessing a distinct phase reserve (PM) and crossover oscillation (fc).

The parallel between this blueprint and the initial one can be observed in Table 1. The fresh configuration shows a lesser amplification at low periodicity and the observed output potential is 448 V, that is, over 10% superior to the delineated figure. (Figure 29).

Table 1. Original design and new design

ORIGINAL DESIGN	NEW DESIGN
Inner loop (type 2) fc=15 kHz PM=60º	Inner loop (type 2) fc=15 kHz PM=60º
External loop (unipolar) fc=25 Hz PM=40º	External loop (unipolar) fc=15 Hz PM=40º
Rated output voltage 400V	Rated output voltage 400V
Actual output voltage 415 V	Actual output voltage 448 V

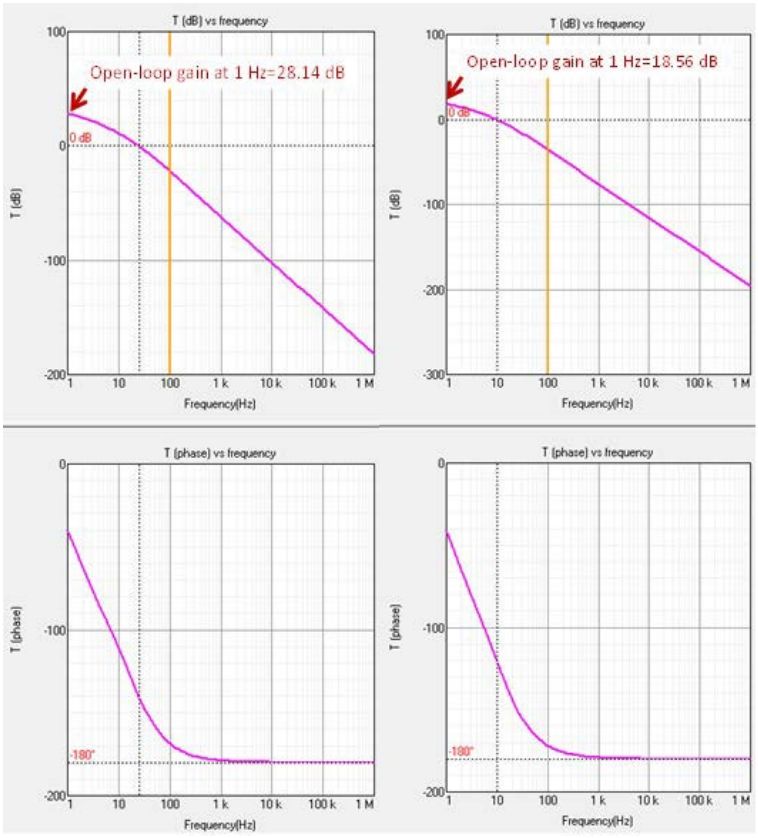

Fig. 29. Low frequency gain with two different designs

Concerning the inner control circuit, it is crucial to deem that one must possess a sufficiently elevated bandwidth to track the rectified sinusoidal setpoint. Should the

crossover frequency of the current circuit be insufficiently high, distortion near zero-crossings will manifest in the input current.

In such instances, the outcomes derived from SmartCtrl might not align with the empirical results, since the line current shape is computed by SmartCtrl presupposing that the current circuit flawlessly follows the setpoint conceived by the outer circuit. [2]

Thus, when zero-crossing distortion is anticipated, the program shows a caution notice to notify the user that the real line current will vary from that depicted. The crossover point of the inner loop compensator ought to be raised to lessen this issue.

To exemplify this challenge linked to the reduced crossover frequency of the inner loop, a contrast among several inner loop setups with varying phase margin (PM) and crossover frequency (f_c) is provided. The input current shapes attained with these configurations are contrasted in Figure 30.

We notice the considerable zero-crossover distortion for crossover frequencies below 5 kHz and how the distortion is diminished as **the crossover frequency grows**. [3], [4], [5], [6], [7]

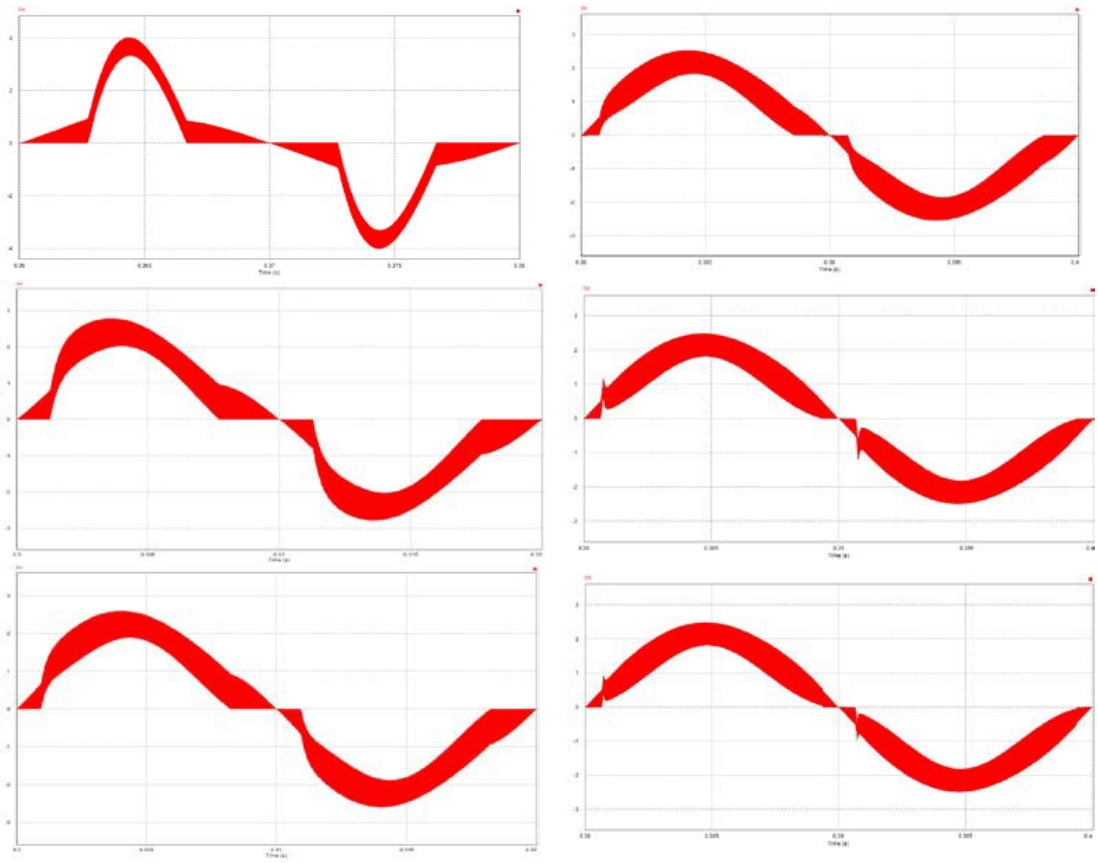

Fig. 30. Zero-crossing distortion with distinct compensators in the current loop

7 Extraction and simulation with PSIM

1. We tap the SmartCtrl export to PSIM button (Figure 31). We set up the export as depicted in Figure 32

Fig. 31. SmartCtrl export to PSIM button

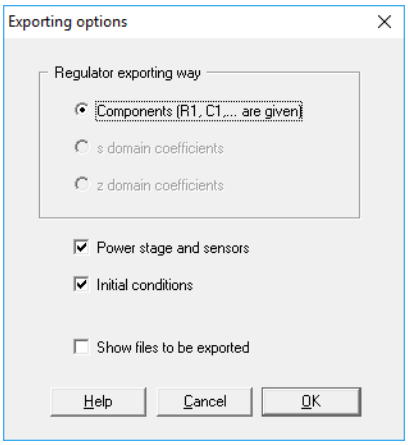

Fig. 32. SmartCtrl export to PSIM options

2. In PSIM, the diagram of Figure 33 will appear, if the simulation is started, the results of Figure 34 will show up

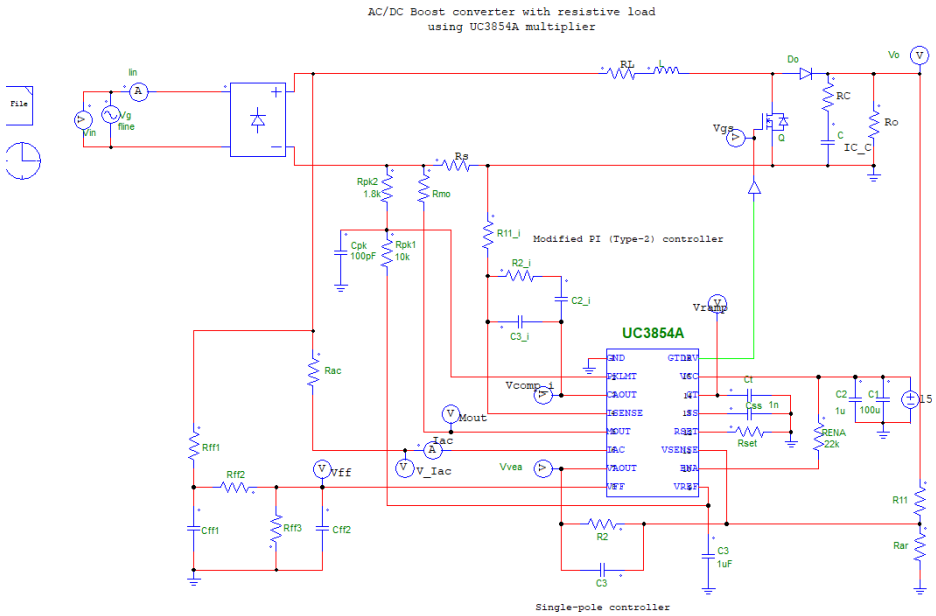

Fig. 33. PSIM Circuit Diagram generated by SmartCtrl

As is observable, the circuit diagram in Figure 33 is precisely the objective of this paper. In Figure 34, the output voltage and the corrected input current are displayed.

As you notice, its current possesses no distortion or ripple and the output voltage is exactly what is stipulated in SmartCtrl.

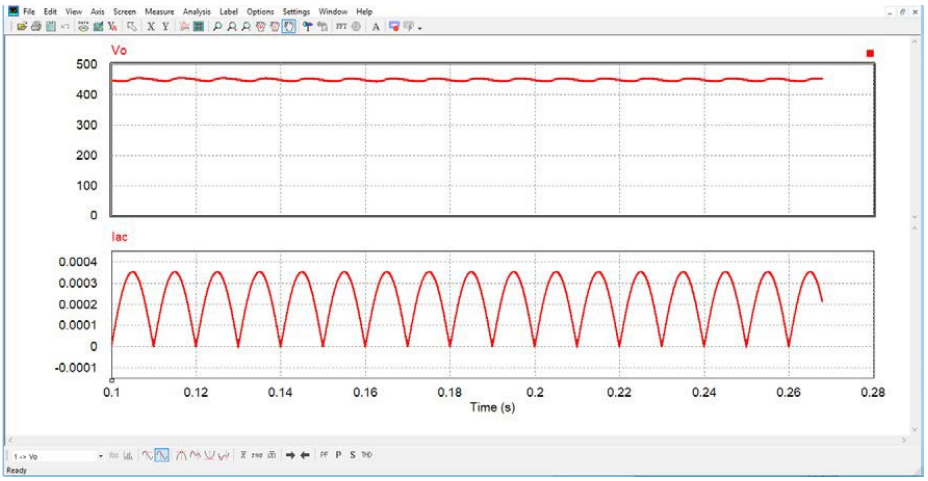

Fig. 34. PSIM simulation waveform

8 Conclusion

Electrical systems suffer a detrimental impact from linear power supplies regarding their power quality. While incorporating passive filters into the power supply offers some enhancement to power quality, it frequently proves insufficient for satisfying established power quality benchmarks. To achieve compliance with these requirements, active power factor correction becomes essential, and a boost PFC converter stands out as one of the most economical and widely adopted methods for deploying such correction.

The operational principle of a boost PFC converter involves employing a switching device to compel the incoming alternating current to exhibit a sinusoidal waveform that remains perfectly aligned in phase with the input voltage. The specific case detailed within this piece demonstrated that the utilization of a boost PFC converter yielded a substantial betterment in the power supply's overall power quality.

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